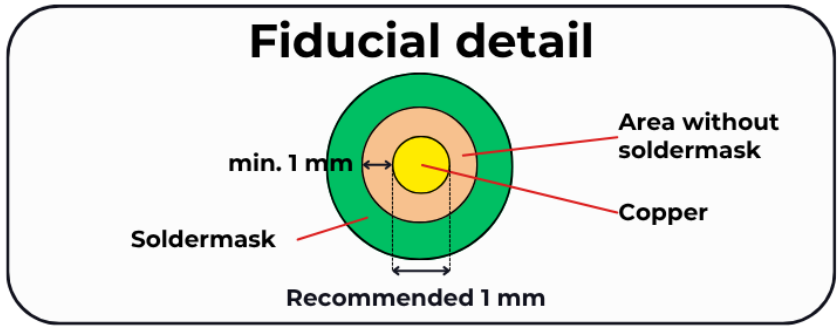

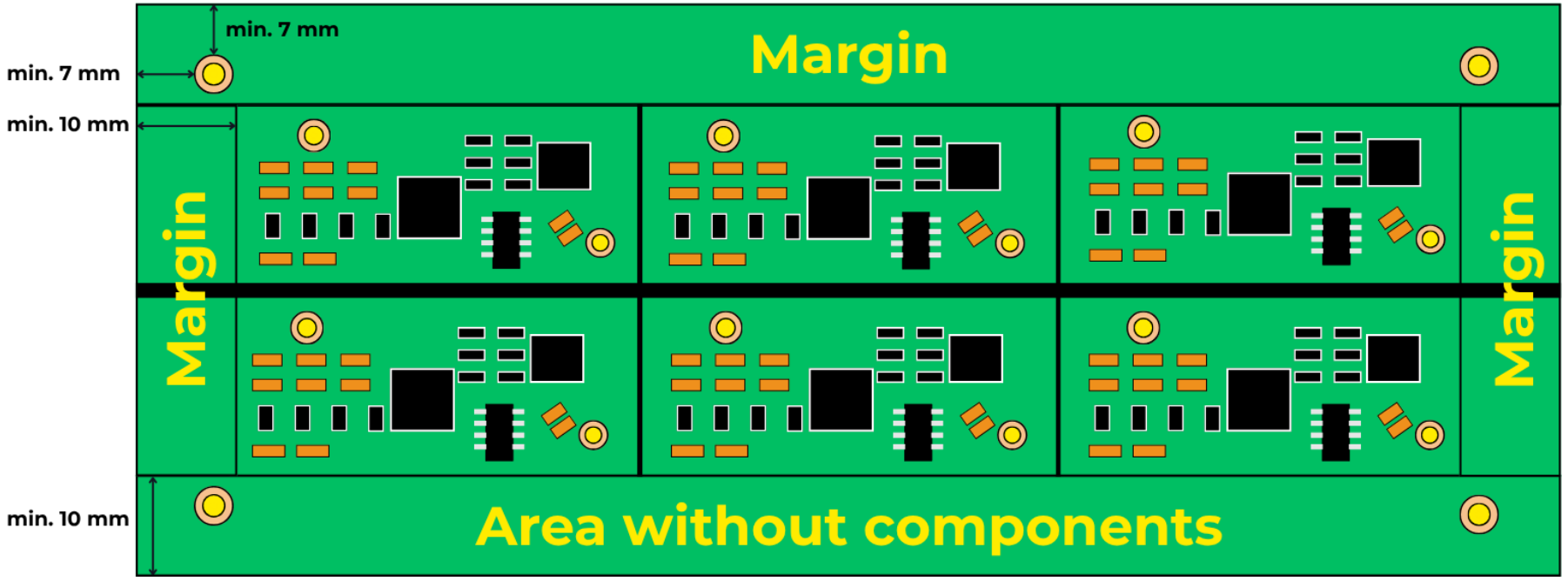

PCB travel direction in reflow oven

1. Purpose and Scope of the Document

This document defines the minimum requirements for preparing PCB designs for the assembly process at ASZ Electronics Solutions. Its purpose is to ensure proper production flow and minimize the risk of assembly and quality issues.

2. Dimensions and Panelization

- Minimum panel size: 120 × 120 mm (length × width),
- Maximum stencil printer working area: 508 × 508 mm (length × width),
- For large double-sided panels, technological rails between panels with a minimum width of 5 mm should be used,
- Additional laminate areas facilitating proper positioning of the panel in production machines should be maintained,
- External rails/margins of at least 10 mm around the panel should be applied.

3. Fiducial Marks

- Panel fiducials must not be symmetrical — they should be offset from the panel edges by at least 5 mm,
- If the customer does not use a panel, the PCB must contain at least two fiducial marks,
- Each panel should contain three fiducials used by assembly machines for coordinate correction,
- Fiducials should be placed at least 7 mm from the panel edge.

4. PCB Technological Requirements

Surface Finish:

- If the PCB contains passive components in 0402 packages or smaller (e.g. 0201, 01005), the surface finish must not be HASL,
- HASL finish should also not be used for components with fine pitch (e.g. 0.05 mm).

Solder Mask:

- The solder mask should be selected according to PCB operating conditions, not for aesthetic reasons,
- Hardness (HB) and resistance to processes such as conformal coating or potting should be considered.

Via-in-Pad Technology:

- Vias located in solder pads must be filled/capped, as open vias may absorb solder during the reflow process, increasing the risk of insufficient solder joints.

Silkscreen Layer:

- Solder barriers should be implemented on the silkscreen layer, especially in areas with high pad density.

Immersion Tin Finish:

- PCBs with immersion tin finish must not be soldered using lead-free solder alloys due to the risk of tin whisker formation,
- This phenomenon does not occur when using leaded solder alloys.

5. Final Notes

Failure to comply with the above guidelines may result in:
- A limitation of the warranty and a downgrade of the IPC assembly class,
- Increased production costs,
- Assembly-related issues.

If there are any doubts regarding production files or panelization, the project should be consulted with the ASZ Electronics Solutions engineering department before being released for production.